Possible Infrastructure Upgrades

- There are changes that can be made to the crate/DAQ infrastructure to increase the bandwidth between the TDC and the event builder. If this is needed, it may be needed regardless of whether or not a new TDC design is built.
  - Add more COT crates to system to reduce number of TDCs/crate and or number of channels/TDC. There is not enough space on the detector for additional crates so this is not feasible.
  - Split the VME backplane into two logical crates each serving 8 TDCs instead of 16
  - Switch to 64 bit transfer instead of 32 bit data transfer
- A possible way of reducing the tails in DSP processing time is to restructure the arrangement of Superlayers in the crate
  - Currently share inner/outer SL within crate
  - Could share inner/outer within a TDC

Split VME Backplanes

- Each crate backplane would be split into two logical crates with 10 or 11 slots each:
  - Each half has its own crate CPU and TRACER
  - Cuts in half bandwidth requirement for VME backplane and TRACER to VRB link (TAXI).
    - Each of these has a capacity of 10-12MB/s.
    - Current occupancy: 2.5kB x 1kHz = 2.5MB/s $\Rightarrow$ could be on the margin in Run IIb

Split Backplanes (cont)

- What hardware resources are needed?
  - Need 20 additional TRACERs
    - Probably enough already since 160 were built for use in about 115 crates
  - Need 20 additional CPUs – buy em
  - Need 2 additional VRBs + Taxi Transition Modules (TART) – enough from spares
  - Slots in crates:
    - If we assume 20 active slots/crate (allows for loss of one slot in making split backplane), have room for 16 TDCs.
    - Currently have 8 crates with 15 TDCs, 10 crates with 16, and 2 crates with 17. Could probably shift a TDC from the 17-slot case to the 15 slot if needed.

Split Backplanes (cont)

- Hardware Resources cont.:
  - Need 20 channels in Trigger/Return XPTs – there are 160 channels. However they are probably not conveniently arranged in a block of 20 or in the same set as existing COT. Will require significant rearrangement
  - Need fiber optic links to TSI, VRB, Ethernet
  - Additional ethernet switch ports, media convertors, clock fanout boards
  - New split backplanes:
    - Would almost certainly buy new crates rather than just backplanes since the Backplane is about 80% of cost of Rittal VIPA crate
    - Now several vendors building VIPA crates
    - Even if split backplane is available from one of these vendors will need a custom design to get bussed CDF trigger/control signals (CDF_CLK, L1A…)
      - **Would do clock/tdc calib differential termination right this time**
    - Might be 2 - 10 slot backplanes or one monolithic backplane

Split Backplane - Cost

		Cost (K$)		
	Qty	Each	Total	Contingency
Crate	25	5	125	50
CPUs	22	4.5	99	9.9
Fibers, Patch Panels	1	19	19	2.9
Ethernet Switch Card	1	10	10	1.5
Clock Fanouts	12	0	0	12
TRACERs	20	0	0	50
Total			253.0	126.3

- Cost of crate is a guess based on cost of previous crates and cost of Minos VME64ext crates from Weiner.
- Expect lead time of about 1 year to procure and test crate
- Need about 1 Month of 3 techs to swap out all 20 crates, install fibers etc

Split Backplane – Other issues

- Regardless of splitting backplanes, it is assumed that FADC boards would be moved from TDC crates to WCAL crates
  - They should be power compatible
  - They have no J3 backplane connector
- If the TDC cards are left in the same order in the crates the new half crates would have larger variation in data size than existing crates
  - The split would typically put all inner layer TDCs within a crate into one side of the split
  - Recabling to interleave these would be a VERY large and painful job
  - This will reduce the possible gains from splitting the backplane

Use Faster VME speed

- The VIPA crates and MVME2301 support VME64, 64 bit transfer multiplexed on 32 data lines
  - This gives a significant improvement in bandwidth
  - The Michigan TDC does not currently support this. The interface chip does and the rest of the board might be made to do so
  - Could also in principle run faster 32bit transfers (factor of 2-3) if the TDC will support
  - TRACER will not support much over 10MB/s and does not support VME64
- Would require a new TRACER design
  - Higher VME bandwidth
  - Different link to VRB (two parallel TAXIs, G-Link…)
  - Could be a Mezannine card for crate CPU to do link to VRB and a retain existing TRACER for interface to Clock/TSI

Re-cabling TDC Input

- This is based on discussions between Jonathan L and Kevin P
- The arrangement of TDCs in COT crates was designed to:
  - Give relatively equal occupancies crate-to-crate by mixing TDCs from inner and outer
  - Allow for cabling of Ansley cables to XFT within the geometry constraints of those cables
  - Minimize ASD to Repeater to TDC cable length
  - Have a single SL in each TDC
  - Increase SL monotonically as move away from TRACER (clock/Calib delays) $\Rightarrow$ even Split blackplanes would violate this
- Limitations on re-cabling include:
  - Very hard to re-cable Ansley's
  - Almost no slack on Input cables to TDC (from Repeaters)
- Idea: combine channels from inner-most layers with ones from outer layer in a single TDC

Re-cabling TDC Input (cont)

- Limited Recabling scheme (only conceptual)
  - In west crates Mix Superlayers 2 and 6 in same TDCs
    ⇒ DSP time = ½ SL2 + ½ SL6
  - In east crates Mix Superlayers 1 and 5 in same TDCs
    ⇒ DSP time = ½ SL1 + ½ SL5 (no effect on Trigger)
- Requires:
  - Swap input cables – Kevin and Jonathan suggest doing this at the repeater card
  - Keep Ansley and input (grey/flat) cable plant intact
  - Replace XFT Ansley receiver transition modules with new ones which handle swap between SL2 and SL6

Re-cabling TDC Input (cont)

- Needed resources:
  - Layout, fabrication and assembly of new XFT transition card (30 cards)
  - Estimate $30-50K parts, fabrication and assembly
  - 1 month senior tech to do layout, ordering + 1/2 month tech for testing
  - Need 1 month of 3 tech for recabling
  - This is a hard job. Don't know for sure that it is possible!

Summary

- Additional bandwidth between TDC and VRB can be achieved but it is not cheap.
- If we undertake a new TDC design, we should seriously consider what the readout architecture should be:
  - support VME64?
  - support other architecture (e.g. PCI)?
- Limited recabling could reduce the DSP processing time by 10-20% with a moderate cost in time and $
- What happened to projective COT?